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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No. 9216

Arthur Ray Alexander, et al.

Group Art Unit: 2841

Serial No.: 09/752,352

Examiner: I. Patel

Filed: 12/29/2000

For: **INTRODUCING LOSS IN A POWER BUS TO REDUCE EMI
AND ELECTRICAL NOISE**Assistant Commissioner for Patents
Washington, D.C. 20231

AMENDMENT

This is a reply to the office action dated December 19, 2001, in this application. Claims 1-19 are pending. Applicant affirms the election of claims 1-8 and 17-19, without traverse. Please cancel the restricted claims (9-16) from the application. Also, please cancel claims 4 and 18 and amend the remaining claims as follows.

1. (Amended) A printed circuit board that includes:
a power layer for use in providing electrical power to circuit components;
a ground layer for use in carrying electrical current away from the circuit components; and
a loss element residing in an internal layer of the circuit board and connected electrically between the power layer and ground layer to suppress electrical noise caused by changes in current flow in the circuit components.

2. (Amended) The circuit board of claim 1, also including a capacitive element connected in series with the loss element.

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By:

Name:

Sallie Spencer

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contd*

3. The circuit board of claim 2, where the loss element and the capacitive element reside in two different layers of the circuit board.

4. Cancelled

5. (Amended) The circuit board of claim 1, where the loss element resides within an internal power or ground plane.

6. The circuit board of claim 1, where the loss element includes a resistor.

7. The circuit board of claim 6, where the resistor has a resistance value on the order of 1-10 ohms.

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8. The circuit board of claim 6, where the resistor is formed from a polymer thick film (PTF) material.

9-16. Cancelled

17. (Amended) A printed circuit board that includes:
electronic circuitry;
a power layer for use in providing electric current to the electronic circuitry; and
a loss element residing within the power layer and connected electrically to the power layer to suppress electrical noise created by sudden changes in current flow in the electronic circuitry.

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18. Cancelled

19. The circuit board of claim 17, where the loss element includes a polymer thick film (PTF) resistor

Please add the following claim.

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20. (New) A printed circuit board comprising multiple layers, including:
at least one layer on which electronic circuitry resides;
at least one power layer for use in providing electric current to the electronic circuitry, comprising:
at least one void formed in the power layer; and
at least one resistive element formed in the void and connected electrically to the power layer to suppress electrical noise created by sudden changes in current flow; and
at least one capacitive element connected in series with the resistive element.

REMARKS

The Examiner has rejected claims 1, 2, 6 and 17 under 35 U.S.C. § 102 (e) and claims 3-5, 7-8 and 18-19 under 35 U.S.C. § 103(a), all in view of Harada. Applicant has amended claims 1 and 17 to include the limitations of original claims 4 and 18, respectively. Applicant has also added claim 20, which includes limitations similar to those found in claims 1 and 17 but is of narrower scope. Support for claim 20 is found in Figures 2 and 3 of Applicant's disclosure and the accompanying text.

As the Examiner concedes in the § 103 rejection, Harada does not show a loss element that resides in an internal layer of a printed circuit board (e.g., within a power or ground plane) to suppress electrical noise caused by sudden changes in current flow. Harada does not even suggest such an element and, in fact, teaches away from an internal loss element of this nature. Harada specifically states that the "series circuit" of capacitors and resistors must be placed between "a top layer power supply pattern and a top layer ground pattern" that are formed around the perimeter of the circuit board's upper layer. (Col. 9, lines 15-28, emphasis added.) Harada does this because he hopes to suppress "an undesired electromagnetic wave" that arises in the circuit board at certain operating frequencies. Forming a band of power and ground traces around the circuitry on the upper layer and placing several R-C circuits along this band is how Harada accomplishes this objective.

Applicant, on the other hand, is attempting to prevent formation of such "undesired electromagnetic waves" altogether. Placing the loss element in an internal layer of the circuit board is not simply a matter of using "the space available" or contributing to "ease of manufacturing," as suggested by the Examiner. Rather, burying the loss element in this manner is the result of Applicant's discovery that placing the loss element nearer to (e.g., within) the power planes greatly reduces circuit inductance and thus inhibits the formation of unwanted electromagnetic waves at higher frequencies than previously possible. Surface-mount and axial-lead components, like those shown on the surface of Harada's board, add circuit inductance and thus narrow the range of frequencies at which EMI suppression occurs. Applicant has also found that loss elements formed from polymer thick-film (PTF) materials are particularly suited for inhibiting EMI at very high frequencies. (See page 4, lines 18-22, of Applicant's disclosure.)

CONCLUSION

Harada does not show or suggest the features of Applicant's claims. The claims are therefore allowable over Harada. Applicant asks the Examiner to reconsider this application and allow all of the claims. Please apply the fee for a two-month extension of time and any other charges that might be due, except the issue fee, to the deposit account 50-1673.

Respectfully submitted,



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